DISPLAY AND METHOD FOR DRIVING DISPLAY

BACKGROUND OF THE INVENTION

Field of the Invention:

The present invention relates to a display apparatus for supplying pixel signals respectively to a plurality of electron emitters arranged in association with a plurality of pixels thereby to display an image, and a method of driving such a display apparatus.

Description of the Related Art:

Recently, electron emitters having a cathode electrode and an anode electrode have been finding use in various applications such as field emission displays (FEDs) and backlight units. In an FED, a plurality of electron emitters are arranged in a two-dimensional array, and a plurality of phosphors are positioned in association with the respective electron emitters with a predetermined gap left therebetween.

Conventional electron emitters are disclosed in the following documents 1 through 5. Various theories about the emission of electrons from a dielectric material making up an emitter have been presented in the following documents 6 through 8:

[Document 1]

Japanese laid-open patent publication No. 1-311533

[Document 2]

Japanese laid-open patent publication No. 7-147131

[Document 3]

Japanese laid-open patent publication No. 2000-285801

[Document 4]

Japanese patent publication No. 46-20944

[Document 5]

Japanese patent publication No. 44-26125

[Document 6]

Yasuoka and Ishii, "Pulsed electron source using a ferroelectric cathode", J. Appl. Phys., Vol. 68, No. 5, p. 546 - 550 (1999)

[Document 7]

V.F. Puchkarev, G.A. Mesyats, On the mechanism of emission from the ferroelectric ceramic cathode, J. Appl. Phys., Vol. 78, No. 9, 1 November, 1995, p. 5633 - 5637

[Document 8]

H. Riege, Electron emission ferroelectrics - a review, Nucl. Instr. and Meth. A340, p. 80 - 89 (1994)

If a display apparatus is constructed using pixels comprising electron emitters, then it is considered to array a number of pixels in a matrix to drive them according to a passive matrix drive process or an active matrix drive process.

For enabling the pixels to emit light, it is necessary to apply a high voltage to the electron emitters. For this reason, for emitting light when the pixels are scanned, it is necessary to apply a high voltage during a period (e.g., one frame) for displaying one image, resulting in the

problem of increased electric power consumption. A circuit for selecting each electron emitter and a circuit for supplying a pixel signal to the selected electron emitter need to be able to handle the high voltage.

The pixels on unselected rows often tend to be affected by a signal that is supplied to the pixels on a selected row, and this leads to an increase in the electric power consumption. Since each pixel is devoid of a memory effect (charge storage at electron emitters), the pixels are disadvantageous in attempts to achieve higher luminance and higher contrast.

SUMMARY OF THE INVENTION

The present invention has been made in view of the above drawbacks. It is an object of the present invention to provide a display apparatus which is designed for low electric power consumption and is capable of being driven at a low voltage, and a method of driving such a display apparatus.

Another object of the present invention is to provide a display apparatus which, in addition to the above capabilities, prevents the pixels on unselected rows from being affected by a signal that is supplied to the pixels on a selected row, and allows each pixel to have a memory effect for higher luminance and higher contrast, and a method of driving such a display apparatus.

A display apparatus according to the present invention

has a plurality of electron emitters arrayed in association with a plurality of pixels, for emitting electrons from the electron emitters to display an image, and is characterized in that necessary charges are accumulated in all the electron emitters in a first period, and a voltage required to emit electrons is applied to all the electron emitters to cause a plurality of electron emitters which correspond to pixels to emit light therefrom, for emitting light from the pixels, in a second period after the first period.

According to the present invention, there is also provided a method of driving a display apparatus having a plurality of electron emitters arrayed in association with a plurality of pixels, for emitting electrons from the electron emitters to display an image, characterized by the step of accumulating necessary charges in all the electron emitters in a first period, and the step of applying a voltage required to emit electrons to all the electron emitters to cause a plurality of electron emitters which correspond to pixels to emit light therefrom, for emitting light from the pixels, in a second period after the first period.

One electron emitter may be assigned to one pixel, or a plurality of electron emitters may be assigned to one pixel.

Usually, if pixels are made up of electron emitters, then a high voltage needs to be applied to the electron emitters to emit light from the pixels. Therefore, for emitting light from the pixels when the pixels are scanned,

a high voltage needs to be applied to the pixels during a period (e.g., one frame) for displaying one image, resulting in the problem of increased electric power consumption. Circuits for selecting electron emitters and supplying pixel signals to the selected electron emitters need to be able to handle the high voltage.

According to the present invention, after charges have been accumulated in all the electron emitters, a voltage is applied to all the electron emitters, emitting light from the pixels which correspond to the electron emitters to be turned on.

Because the period (first period) for accumulating charges in electron emitters and the period (second period) for emitting electrons from electron emitters which correspond to the pixels to be turned on are separated from each other, the circuit for applying voltages (an accumulation voltage and an emission voltage) depending on luminance levels to the electron emitters can be driven at a low voltage.

Specific drive methods for driving the display apparatus according to the present invention will be described below.

According to a first drive method, one image is displayed in a period as one frame, the one frame including the first period and the second period, all the electron emitters are scanned, and accumulation voltages depending on the luminance levels of corresponding pixels are applied to

the electron emitters which correspond to pixels to emit light therefrom in the first period, to accumulate charges in amounts depending on the luminance levels of corresponding pixels in the electron emitters which correspond to pixels to emit light therefrom in the first period, and a constant emission voltage is applied to all the electron emitters in the second period after the first period, to emit electrons in amounts depending on the luminance levels of corresponding pixels from the electron emitters which correspond to pixels to emit light therefrom in the second period, thereby emitting light from the pixels.

According to a second drive method, one image is displayed in a period as one frame, the one frame being divided into a plurality of periods having respective different luminance levels, each of the periods serving as one subfield, the one subfield including the first period and the second period, all the electron emitters are scanned, and a constant accumulation voltage is applied to the electron emitters to emit light therefrom in the first period, to accumulate a constant amount of charges in the electron emitters to emit light therefrom in the first period, and emission voltages depending on luminance levels assigned to the subfields are applied to all the electron emitters in the second period after the first period, to emit electrons in amounts depending on the luminance levels assigned to the subfields from the electron emitters which

correspond to pixels to emit light therefrom in the second period, thereby emitting light from the pixels.

According to a third drive method, one image is displayed in a period as one frame, the one frame being divided into a plurality of periods having respective different luminance levels, each of the periods serving as one subfield, the one subfield including the first period and the second period, all the electron emitters are scanned, and accumulation voltages depending on luminance levels assigned to the subfields are applied to the electron emitters to emit light therefrom in the first period, to accumulate charges in amounts depending on the luminance levels assigned to the subfields in the electron emitters to emit light therefrom in the first period, and a constant emission voltage is applied to all the electron emitters in the second period after the first period, to emit electrons in amounts depending on the luminance levels assigned to the subfields from the electron emitters which correspond to pixels to emit light therefrom in the second period, thereby emitting light from the pixels.

According to a fourth drive method, one image is displayed in a period as one frame, the one frame being divided into a plurality of periods having the same luminance level, each of the periods serving as one linear subfield, the one linear subfield including the first period and the second period, all the electron emitters are scanned, and a constant accumulation voltage is applied to

the electron emitters to emit light therefrom in the liner subfields in the first period, to accumulate a constant amount of charges in the electron emitters to emit light therefrom in the linear subfields in the first period, and a constant emission voltage is applied to all the electron emitters in the second period after the first period, to emit a constant amount of electrons from the electron emitters which correspond to pixels to emit light therefrom in the linear subfields in the second period, thereby emitting light from the pixels.

According to a fifth drive method, one image is displayed in a period as one frame, the one frame including the first period and the second period, a constant accumulation voltage is applied to all the electron emitters in the first period to accumulate a constant amount of charges in all the electron emitters in the first period, and all the electron emitters are scanned and emission voltages depending on the luminance levels of corresponding pixels are applied to the electron emitters which correspond to pixels to emit light therefrom in the second period after the first period, to emit electrons in amounts depending on the luminance levels of corresponding pixels from the electron emitters which correspond to pixels to emit light therefrom in the second period, thereby emitting light from the pixels.

According to a sixth drive method, one image is displayed in a period as one frame, the one frame being

divided into a plurality of periods having respective different luminance levels, each of the periods serving as one subfield, the one subfield including the first period and the second period, accumulation voltages depending on luminance levels assigned to the subfields are applied to all the electron emitters to emit light therefrom in the first period, to accumulate charges in amounts depending on the luminance levels assigned to the subfields in all the electron emitters in the first period, and all the electron emitters are scanned and a constant emission voltage is applied to the electron emitters to emit light therefrom in the second period after the first period, to emit electrons in amounts depending on the luminance levels assigned to the subfields from the electron emitters which correspond to pixels to emit light therefrom in the second period, thereby emitting light from the pixels.

According to a seventh drive method, one image is displayed in a period as one frame, the one frame being divided into a plurality of periods having respective different luminance levels, each of the periods serving as one subfield, the one subfield including the first period and the second period, a constant accumulation voltage is applied to all the electron emitters in the first period, to accumulate a constant amount of charges in all the electron emitters in the first period, and all the electron emitters are scanned emission voltages depending on the luminance levels assigned to the subfields are applied to the electron

emitters to emit light therefrom in the second period after the first period, to emit electrons in amounts depending on the luminance levels assigned to the subfields from the electron emitters which correspond to pixels to emit light therefrom in the second period, thereby emitting light from the pixels.

According to an eighth drive method, one image is displayed in a period as one frame, the one frame being divided into a plurality of periods having the same luminance level, each of the periods serving as one linear subfield, the one linear subfield including the first period and the second period, a constant accumulation voltage is applied to all the electron emitters in the first period, to accumulate a constant amount of charges in the electron emitters to emit light therefrom in the linear subfields in the first period, and all the electron emitters are scanned and a constant emission voltage is applied to the electron emitters to emit light therefrom in the linear subfields in the second period after the first period, to emit a constant amount of electrons from the electron emitters which correspond to pixels to emit light therefrom in the linear subfields in the second period, thereby emitting light from the pixels.

In the above drive methods, particularly, in the first, third, fourth, and sixth drive methods, a pulse signal having a constant pulse amplitude may be generated, and the pulse signal may be amplitude-modulated to generate the

accumulation voltage in the first period. Alternatively, a pulse signal applicable to the electron emitters may be generated, the pulse signal having a voltage waveform including a positive-going edge or a negative-going edge which is continuously variable in level, and the pulse signal may be pulse-width-modulated to generate the accumulation voltage in the first period.

In the above drive methods, particularly, in the second, fifth, seventh, and eighth drive methods, a pulse signal having a constant pulse amplitude may be generated, and the pulse signal may be amplitude-modulated to generate the emission voltage in the second period. Alternatively, a pulse signal applicable to the electron emitters may be generated, the pulse signal having a voltage waveform including a positive-going edge or a negative-going edge which is continuously variable in level, and the pulse signal may be pulse-width-modulated to generate the emission voltage in the second period.

If the electron emitters that are used have such characteristics that the electron emitters change to a state (first state) in which electrons are accumulated when an electric field is applied in one direction to the electron emitters, and change from the first state to a state (second state) in which electrons are emitted when an electric field is applied in another direction to the electron emitters, then it is preferable to apply a voltage between a voltage for changing the electron emitters to the first state and a

voltage for changing the electron emitters to a state immediately prior to the second state, to electron emitters which are unselected. With such an arrangement, unselected pixels are not affected by signals supplied to selected pixels, and a memory effect can be achieved at each pixel for higher luminance and higher contrast.

With the display apparatus and the method of driving the display apparatus according to the present invention, as described above, the display apparatus can have low power consumption and can be driven at a low voltage.

Furthermore, unselected pixels are not affected by signals supplied to selected pixels, and a memory effect can be achieved at each pixel for higher luminance and higher contrast.

The above and other objects, features, and advantages will become apparent from the following description of the preferred embodiments when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a display area and a drive circuit of a display apparatus according to an embodiment of the present invention;

FIGS. 2A through 2C are waveform diagrams illustrative of the amplitude modulation of pulse signals by an amplitude modulating circuit;

FIG. 3 is a block diagram of a signal supply circuit

according to a modification;

FIGS. 4A through 4C are waveform diagrams illustrative of the pulse width modulation of pulse signals by a pulse width modulating circuit;

FIG. 5 is a diagram showing the voltage vs. charge quantity characteristics (voltage vs. polarized quantity characteristics) of an electron emitter used in the display apparatus according to the embodiment of the present invention;

FIG. 6 is a fragmentary cross-sectional view of an electron emitter used in the display apparatus according to the embodiment of the present invention;

FIG. 7 is an enlarged fragmentary cross-sectional view of the electron emitter;

FIG. 8 is a plan view showing an example of the shape of through regions defined in an upper electrode;

FIG. 9 is a view showing a layout of a collector electrode, a phosphor, and a transparent plate on the upper electrode;

FIG. 10 is a view showing another layout of a collector electrode, a phosphor, and a transparent plate on the upper electrode;

FIG. 11A is a view illustrative of a state at a point p1 shown in FIG 5;

FIG. 11B is a view illustrative of a state at a point p2 shown in FIG 5;

FIG. 11C is a view illustrative of a state from the

point p2 to a point p3 shown in FIG 5;

FIG. 12A is a view illustrative of a state from the point p3 to a point p4 shown in FIG 5;

FIG. 12B is a view illustrative of a state immediately prior to a point p4 shown in FIG. 5;

FIG. 12C is a view illustrative of a state from the point p4 to a point p6 shown in FIG 5;

FIG. 13A is a diagram showing a hysteresis curve plotted when a voltage Vsl shown in FIG. 2A or 4A is applied;

FIG. 13B is a diagram showing a hysteresis curve plotted when a voltage Vsm shown in FIG. 2B or 4B is applied;

FIG. 13C is a diagram showing a hysteresis curve plotted when a voltage Vsh shown in FIG. 2C or 4C is applied;

FIG. 14A is a diagram showing the waveform of a write pulse and a turn-on pulse that are used in a first experimental example (an experiment for observing the emission of electrons from an electron emitter);

FIG. 14B is a diagram showing the waveform of a detected voltage of a light-detecting device, which is representative of the emission of electrons from the electron emitter in the first experimental example;

FIG. 15 is a diagram showing the waveform of a write pulse and a turn-on pulse that are used in first through fourth experimental examples;

FIG. 16 is a characteristic diagram showing the results of a second experimental example (an experiment for observing how the amount of electrons emitted from the electron emitter changes depending on the amplitude of a write pulse);

FIG. 17 is a characteristic diagram showing the results of a third experimental example (an experiment for observing how the amount of electrons emitted from the electron emitter changes depending on the amplitude of a turn-on pulse);

FIG. 18 is a characteristic diagram showing the results of a fourth experimental example (an experiment for observing how the amount of electrons emitted from the electron emitter changes depending on the level of a collector voltage);

FIG. 19 is a view showing a cross-sectional shape of an overhanging portion of the upper electrode of the electron emitter;

FIG. 20 is a view showing a cross-sectional shape of another overhanging portion of the upper electrode of the electron emitter;

FIG. 21 is a view showing a cross-sectional shape of still another overhanging portion of the upper electrode of the electron emitter;

FIG. 22 is an equivalent circuit diagram showing a connected state of various capacitors connected between an upper electrode and a lower electrode;

FIG. 23 is a diagram illustrative of calculations of capacitances of the various capacitors connected between the upper electrode and the lower electrode;

FIG. 24 is a fragmentary plan view of an electron emitter according to a first modification of the embodiment;

FIG. 25 is a fragmentary plan view of an electron emitter according to a second modification of the embodiment;

FIG. 26 is a fragmentary plan view of an electron emitter according to a third modification of the embodiment;

FIG. 27 is a timing chart illustrative of a first drive method;

FIG. 28 is a diagram showing the relationship of applied voltages according to the first drive method;

FIG. 29 is a timing chart illustrative of a second drive method;

FIG. 30 is a block diagram of a signal supply circuit used in the second drive method;

FIG. 31 is a diagram showing the relationship of applied voltages according to the second drive method;

FIG. 32 is a timing chart illustrative of a third drive method;

FIG. 33 is a diagram showing the relationship of applied voltages according to the third drive method;

FIG. 34 is a timing chart illustrative of a fourth drive method;

FIG. 35 is a block diagram of a signal supply circuit

used in the fourth drive method;

FIG. 36 is a diagram showing the relationship of applied voltages according to the fourth drive method;

FIG. 37 is a timing chart illustrative of a fifth drive method;

FIG. 38 is a block diagram of a row selecting circuit and a signal supplying circuit used in the fifth drive method;

FIG. 39 is a diagram showing the relationship of applied voltages according to the fifth drive method;

FIG. 40 is a timing chart illustrative of a sixth drive method;

FIG. 41 is a diagram showing the relationship of applied voltages according to the sixth drive method;

FIG. 42 is a timing chart illustrative of a seventh drive method;

FIG. 43 is a diagram showing the relationship of applied voltages according to the seventh drive method;

FIG. 44 is a timing chart illustrative of an eighth drive method; and

FIG. 45 is a diagram showing the relationship of applied voltages according to the eighth drive method.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Display apparatus and methods of driving same according to embodiments of the present invention will be described below with reference to FIGS. 1 through 45.

As shown in FIG. 1, a display apparatus 10 according to an embodiment of the present invention has a display unit 14 comprising a matrix or staggered pattern of electron emitters 10 corresponding to respective pixels, and a drive circuit 16 for driving the display unit 14. One electron emitter 12 may be assigned to each pixel, or a plurality of electron emitters 12 may be assigned to each pixel. In the present embodiment, it is assumed for the sake of brevity that one electron emitter 12 is assigned to each pixel.

The drive circuit 16 has a plurality of row select lines 18 for selecting rows in the display unit 14 and a plurality of signal lines 20 for supplying pixel signals Sd to the display unit 14.

The drive circuit 16 also has a row selecting circuit 22 for supplying a selection signal Ss selectively to the row select lines 18 to successively select a row of electron emitters 12, a signal supplying circuit 24 for outputting parallel pixel signals Sd to the signal lines 20 to supply the pixel signals Sd to a row (selected row) selected by the row selecting circuit 22, and a signal control circuit 26 for controlling the row selecting circuit 22 and the signal supplying circuit 24 based on a video signal Sv and a synchronizing signal Sc that are input to the signal control circuit 26.

A power supply circuit 28 (which supplies 50 V and 0 V, for example) is connected to the row selecting circuit 22 and the signal supplying circuit 24. A pulse power supply

30 is connected between a negative line between the row selecting circuit 22 and the power supply circuit 28, and GND (ground). The pulse power supply 30 outputs a pulsed voltage waveform having a reference voltage (e.g., 0 V) during a charge accumulation period Td, to be described later, and a certain voltage (e.g., - 400 V) during a light emission period Th.

During the charge accumulation period Td, the row selecting circuit 22 outputs the selection signal Ss to the selected row and outputs a non-selection signal Sn to the unselected rows. During the light emission period Th, the row selecting circuit 22 outputs a constant voltage (e.g., - 350 V) which is the sum of a power supply voltage (e.g., 50 V) from the power supply circuit 28 and a voltage (e.g., - 400 V) from the pulse power supply 30.

The signal supplying circuit 24 has a pulse generating circuit 32 and an amplitude modulating circuit 34. The pulse generating circuit 32 generates a pulse signal Sp having a constant pulse period and a constant amplitude (e.g., 50 V) during the charge accumulation period Td, and outputs a reference voltage (e.g., 0 V) during the light emission period Th.

During the charge accumulation period Td, the amplitude modulating circuit 34 amplitude-modulates the pulse signal Sp from the pulse generating circuit 32 depending on the luminance levels of the pixels of the selected row, and outputs the amplitude-modulated pulse signal Sp as the pixel

signal for the pixels Sd of the selected row. During the light emission period Th, the amplitude modulating circuit 34 outputs the reference voltage from the pulse generating circuit 32 as it is. The timing control in the amplitude modulating circuit 34 and the supply of the luminance levels of the selected pixels to the amplitude modulating circuit 34 are performed by the signal control circuit 26.

For example, as indicated by three examples shown in FIGS. 2A through 2C, if the luminance level is low, then the amplitude of the pulse signal Sp is set to a low level Vsl (see FIG. 2A), if the luminance level is medium, then the amplitude of the pulse signal Sp is set to a medium level Vsm (see FIG. 2B), and if the luminance level is high, then the amplitude of the pulse signal Sp is set to a high level Vsh (see FIG. 2C). Though the amplitude of the pulse signal Sp is modulated into three levels in the above examples, if the amplitude modulation is applied to the display apparatus 10, then the pulse signal Sp is amplitude-modulated to 128 levels or 256 levels depending on the luminance levels of the pixels.

A modification of the signal supplying circuit 24 will be described below with reference to FIGS. 3 through 4C.

As shown in FIG. 3, a modified signal supplying circuit 24a has a pulse generating circuit 36 and a pulse width modulating circuit 38. The pulse generating circuit 36 generates and outputs a pulse signal Spa (indicated by the broken lines in FIGS. 4A through 4C) where the positive-

going edge of a voltage waveform (indicated by the solid lines in FIGS. 4A through 4C) applied to the electron emitter 12 is continuously changed in level, during the charge accumulation period Td. The pulse generating circuit 36 outputs a reference voltage during the light emission period Th. During the charge accumulation period Td, the pulse width modulating circuit 38 modulates the pulse width Wp (see FIGS. 4A through 4C) of the pulse signal Spa from the pulse generating circuit 36 depending on the luminance levels of the pixels of the selected row, and outputs the pulse signal Spa with the modulated pulse width Wp as the pixel signal Sd for the pixels of the selected row. During the light emission period Th, the pulse width modulating circuit 38 outputs the reference voltage from the pulse generating circuit 36 as it is. The timing control in the pulse width modulating circuit 38 and the supply of the luminance levels of the selected pixels to the pulse with modulating circuit 38 are also performed by the signal control circuit 26.

For example, as indicated by three examples shown in FIGS. 4A through 4C, if the luminance level is low, then the pulse width p of the pulse signal Sp is set to a short width, setting the substantial amplitude to a low level Vsl (see FIG. 4A), if the luminance level is medium, then the pulse width Wp of the pulse signal Sp is set to a medium width, setting the substantial amplitude to a medium level Vsm (see FIG. 4B), and if the luminance level is high, then

the pulse width Wp of the pulse signal Sp is set to a long width, setting the substantial amplitude to a high level Vsh (see FIG. 4C). Though the pulse width Wp of the pulse signal Sp is modulated into three levels in the above examples, if the amplitude modulation is applied to the display apparatus 10, then the pulse signal Sp is pulse-width-modulated to 128 levels or 256 levels depending on the luminance levels of the pixels.

Preferable characteristics of the electron emitter 12 will be described below. The electron emitter 12 has an electron emission region (a region from which electrons are emitted) characterized by an asymmetric hysteresis curve based on the reference voltage = 0 (V) in vacuum, as indicated by the voltage vs. charge quantity characteristics shown in FIG. 5.

The voltage vs. charge quantity characteristics will be described below. At a point p1 (initial state) where the reference voltage is applied, almost no electrons are stored in the electron emission region. Thereafter, when a negative voltage is applied, the amount of positive charges in the electron emission region increases, storing electrons. When the level of the negative voltage increases in a negative direction, electrons are progressively stored in the electron emission region until the amount of positive charges and the amount of electrons are held in equilibrium with each other at a point p2 of the negative voltage. As the level of the negative voltage further increases in the

negative direction, the stored amount of electrons increases, making the amount of negative charges greater than the amount of positive charges. The accumulation of electrons is saturated at a point P3.

As the level of the negative voltage further increases, and a positive voltage is applied in excess of the reference voltage, electrons start being emitted at a point p4. When the positive voltage increases in a positive direction, the amount of emitted electrons increases until the amount of positive charges and the amount of electrons are held in equilibrium with each other at a point p5. At a point p6, almost all the stored electrons are emitted, bringing the difference between the amount of positive charges and the amount of negative charges into substantial conformity with a value in the initial state.

The voltage vs. charge quantity characteristics have the following features:

(1) If the negative voltage at the point p2 where the amount of positive charges and the amount of electrons are held in equilibrium with each other is represented by V1 and the positive voltage at the point p5 by V2, then these voltages satisfy the following relationship:

$|V1| < |V2|$

(2) More specifically, the relationship is expressed as $1.5 \times |V1| < |V2|$

(3) If the rate of change of the amount of positive charges and the amount of electrons at the point p2 is

represented by $\Delta Q1/\Delta V1$ and the rate of change of the amount of positive charges and the amount of electrons at the point p5 by $\Delta Q2/\Delta V2$, then these rates satisfy the following relationship:

$$(\Delta Q1/\Delta V1) > (\Delta Q2/\Delta V2)$$

(4) If the voltage at which the accumulation of electrons is saturated is represented by V3 and the voltage at which electrons start being emitted by V4, then these voltages satisfy the following relationship:

$$1 \leq |V4|/|V3| \leq 1.5$$

An example of electron emitter 12 which satisfy the above characteristics will be described below with reference to FIGS. 6 through 26.

As shown in FIG. 6, the electron emitter 12 comprises a plate-like emitter (a substance serving as an emitter) 40 made of a dielectric material, an upper electrode 42 formed on an upper surface, for example, of the emitter 40 and connected to a signal line 20, and a lower electrode 44 formed on a lower surface, for example, of the emitter 40 and connected to a row select line 18. In this embodiment, the signal line 20 is connected to the upper electrode 42, and the row select line 18 is connected to the lower electrode 44. Conversely, the row select line 18 may be connected to the upper electrode 42, and the signal line 20 may be connected to the lower electrode 44.

The upper electrode 42 has a plurality of through regions 46 where the emitter 40 is exposed. The emitter 40

has surface irregularities 48 due to the grain boundary of the dielectric material. The through regions 46 of the upper electrode 42 are formed in areas corresponding to concavities 50 due to the grain boundary of the dielectric material. In the embodiment shown in FIG. 6, one through region 46 is formed in association with one recess 50. However, one through region 46 may be formed in association with a plurality of concavities 50. The particle diameter of the dielectric material of the emitter 40 should preferably be in the range from 0.1 µm to 10 µm, and more preferably be in the range from 2 µm to 7 µm. In the embodiment shown in FIG. 6, the particle diameter of the dielectric material is of 3 µm.

In this embodiment, as shown in FIG. 7, each of the through regions 46 of the upper electrode 42 has a peripheral portion 52 having a surface 52a facing the emitter 40, the surface 52a being spaced from the emitter 40. Specifically, a gap 54 is formed between the surface 52a, facing the emitter 40, of the peripheral portion 52 of the through region 46 and the emitter 40, and the peripheral portion 52 of the through region 46 of the upper electrode 42 is formed as an overhanging portion (flange). In the description which follows, "the peripheral portion 52 of the through region 46 of the upper electrode 42" is referred to as "the overhanging portion 52 of the upper electrode 42". In FIGS. 6, 7, 9, 10, 11A through 11C, 12A through 12C, 19 through 21, and 26, convexities 56 of the surface

irregularities 48 of the grain boundary of the dielectric material are shown as having a semicircular cross-sectional shape. However, the convexities 56 are not limited to the semicircular cross-sectional shape.

With the electron emitter 12, the upper electrode 42 has a thickness t in the range of $0.01\ \mu m \le t \le 10\ \mu m$, and the maximum angle θ between the upper surface of the emitter 40, i.e., the surface of the convexity 56 (which is also the inner wall surface of the concavity 50) of the grain boundary of the dielectric material, and the lower surface 56a of the overhanging portion 52 of the upper electrode 42 is in the range of $1° \le \theta \le 60°$. The maximum distance d in the vertical direction between the surface of the convexity 56 (the inner wall surface of the concavity 50) of the grain boundary of the dielectric material and the lower surface 56a of the overhanging portion 52 of the upper electrode 42 is in the range of $0\ \mu m < d \le 10\ \mu m$.

In the electron emitter 12, the shape of the through region 46, particularly the shape as seen from above, as shown in FIG. 8, is the shape of a hole 58, which may be a circular shape, an elliptical shape, a track shape, a shape including a curve, or a polygonal shape such as a quadrangular shape or a triangular shape. In FIG. 8, the shape of the hole 58 is a circular shape.

The hole 58 has an average diameter ranging from 0.1 µm to 10 µm. The average diameter represents the average of the lengths of a plurality of different line segments

passing through the center of the hole 58.

Materials of the various components will be described below. The dielectric material which the emitter 40 is made of may be a dielectric material having a relatively high dielectric constant, e.g., a dielectric constant of 1000 or higher. Dielectric materials of such a nature may be ceramics including barium titanate, lead zirconate, lead magnesium niobate, lead nickel niobate, lead zinc niobate, lead manganese niobate, lead magnesium tantalate, lead antimony tinate, lead titanate, lead magnesium tungstenate, lead cobalt niobate, etc. or a combination of any of these materials, a material which chiefly contains 50 weight % or more of any of these materials, or such ceramics to which there is added an oxide such as lanthanum, calcium, strontium, molybdenum, tungsten, barium, niobium, zinc, nickel, manganese, or the like, or a combination of these materials, or any of other compounds.

For example, a two-component material nPMN-mPT (n, m represent molar ratios) of lead magnesium niobate (PMN) and lead titanate (PT) has its Curie point lowered for a larger specific dielectric constant at room temperature if the molar ratio of PMN is increased.

Particularly, a dielectric material where n = 0.85 - 1.0 and m = 1.0 - n is preferable because its specific dielectric constant is 3000 or higher. For example, a dielectric material where n = 0.91 and m = 0.09 has a specific dielectric constant of 15000 at room temperature,

and a dielectric material where n = 0.95 and m = 0.05 has a specific dielectric constant of 20000 at room temperature.

For increasing the specific dielectric constant of a three-component dielectric material of lead magnesium niobate (PMN), lead titanate (PT), and lead zirconate (PZ), it is preferable to achieve a composition close to a morphotropic phase boundary (MPB) between a tetragonal system and a quasi-cubic system or a tetragonal system and a rhombohedral system, as well as to increase the molar ratio of PMN. For example, a dielectric material where PMN : PT : PZ = 0.375 : 0.375 : 0.25 has a specific dielectric constant of 5500, and a dielectric material where PMN : PT : PZ = 0.5 : 0.375 : 0.125 has a specific dielectric constant of 4500, which is particularly preferable. Furthermore, it is preferable to increase the dielectric constant by introducing a metal such as platinum into these dielectric materials within a range to keep them insulative. For example, a dielectric material may be mixed with 20 weight % of platinum.

The emitter 40 may be in the form of a piezoelectric/electrostrictive layer or an anti-ferroelectric layer. If the emitter 40 comprises a piezoelectric/electrostrictive layer, then it may be made of ceramics such as lead zirconate, lead magnesium niobate, lead nickel niobate, lead zinc niobate, lead manganese niobate, lead magnesium tantalate, lead nickel tantalate, lead antimony tinate, lead titanate, barium titanate, lead

magnesium tungstenate, lead cobalt niobate, or the like. or a combination of any of these materials.

The emitter 40 may be made of chief components including 50 wt % or more of any of the above compounds. Of the above ceramics, the ceramics including lead zirconate is mostly frequently used as a constituent of the piezoelectric/electrostrictive layer of the emitter 40.

If the piezoelectric/electrostrictive layer is made of ceramics, then lanthanum, calcium, strontium, molybdenum, tungsten, barium, niobium, zinc, nickel, manganese, or the like, or a combination of these materials, or any of other compounds may be added to the ceramics. Alternatively, ceramics produced by adding SiO_2, CeO_2, $Pb_5Ge_3O_{11}$, or a combination of any of these compounds to the above ceramics may be used. Specifically, a material produced by adding 0.2 wt % of SiO_2, 0.1 wt % of CeO_2, or 1 to 2 wt % of $Pb_5Ge_3O_{11}$ to a PT-PZ-PMN piezoelectric material is preferable.

For example, the piezoelectric/electrostrictive layer should preferably be made of ceramics including as chief components lead magnesium niobate, lead zirconate, and lead titanate, and also including lanthanum and strontium.

The piezoelectric/electrostrictive layer may be dense or porous. If the piezoelectric/electrostrictive layer is porous, then it should preferably have a porosity of 40 % or less.

If the emitter 40 is in the form of an anti-

ferroelectric layer, then the anti-ferroelectric layer may be made of lead zirconate as a chief component, lead zirconate and lead tin as chief components, lead zirconate with lanthanum oxide added thereto, or lead zirconate and lead tin as components with lead zirconate and lead niobate added thereto.

The anti-ferroelectric layer may be porous. If the anti-ferroelectric layer is porous, then it should preferably have a porosity of 30 % or less.

If the emitter 40 is made of strontium tantalate bismuthate ($SrBi_2Ta_2O_9$), then its polarization reversal fatigue is small. Materials whose polarization reversal fatigue is small are laminar ferroelectric compounds and expressed by the general formula of $(BiO_2)^{2+}(A_{m-1}B_mO_{3m+1})^{2-}$. Ions of the metal A are Ca^{2+}, Sr^{2+}, Ba^{2+}, Pb^{2+}, Bi^{3+}, La^{3+}, etc., and ions of the metal B are Ti^{4+}, Ta^{5+}, Nb^{5+}, etc.

The baking temperature can be lowered by adding glass such as lead borosilicate glass or the like or other compounds of low melting point (e.g., bismuth oxide or the like) to the piezoelectric/electrostrictive/anti-ferroelectric ceramics.

If the emitter 40 is made of piezoelectric/electrostrictive/anti-ferroelectric ceramics, then it may be a sheet-like molded body, a sheet-like laminated body, or either one of such bodies stacked or bonded to another support substrate.

If the emitter 40 is made of a non-lead-based material,

then it may be a material having a high melting point or a high evaporation temperature so as to be less liable to be damaged by the impingement of electrons or ions.

The upper electrode 42 is made of an organic metal paste which can produce a thin film after being baked. For example, a platinum resinate paste or the like, should preferably be used. An oxide electrode for suppressing a polarization reversal fatigue, which is made of ruthenium oxide (RuO_2), iridium oxide (IrO_2), strontium ruthenate ($SrRuO_3$), $La_{1-x}Sr_xCoO_3$ (e.g., x = 0.3 or 0.5), $La_{1-x}Ca_xMnO_3$, (e.g., x = 0.2), $La_{1-x}Ca_xMn_{1-y}Co_yO_3$ (e.g., x = 0.2, y = 0.05), or a mixture of any one of these compounds and a platinum resinate paste, for example, is preferable.

The upper electrode 42 may be made of any of the above materials by any of thick-film forming processes including screen printing, spray coating, coating, dipping, electrophoresis, etc., or any of various thin-film forming processes including sputtering, an ion beam process, vacuum evaporation, ion plating, chemical vapor deposition (CVD), plating, etc. Preferably, the upper electrode 42 is made by any of the above thick-film forming processes.

The lower electrode 44 is made of platinum, molybdenum, tungsten, or the like. Alternatively, the lower electrode 44 is made of an electric conductor which is resistant to a high-temperature oxidizing atmosphere, e.g., a metal, an alloy, a mixture of insulative ceramics and a metal, a mixture of insulative ceramics and an alloy, or the like.

Preferably, the lower electrode 44 should be made of a precious metal having a high melting point such as platinum, iridium, palladium, rhodium, molybdenum, or the like, or a material chiefly composed of an alloy of silver and palladium, silver and platinum, platinum and palladium, or the like, or a cermet of platinum and ceramics. Further preferably, the lower electrode 44 should be made of platinum only or a material chiefly composed of a platinum-base alloy.

The lower electrode 44 may be made of carbon or a graphite-base material. Ceramics to be added to the electrode material should preferably have a proportion ranging from 5 to 30 volume %. The lower electrode 44 may be made of the same material as the upper electrode, as described above.

The lower electrode 44 should preferably be formed by any of various thick-film forming processes. The lower electrode 44 has a thickness of 20 μm or less or preferably a thickness of 5 μm or less.

Each time the emitter 40, the upper electrode 42, or the lower electrode 44 is formed, the assembly is heated (sintered) into an integral structure.

The sintering process for integrally combining the emitter 40, the upper electrode 42, and the lower electrode 44 may be carried out at a temperature ranging from 500 to 1400°c, preferably from 1000 to 1400°C. For heating the emitter 40 which is in the form of a film, the emitter 40

should be sintered together with its evaporation source while their atmosphere is being controlled, so that the composition of the emitter 40 will not become unstable at high temperatures.

By performing the sintering process, the film which will serve as the upper electrode 42 is shrunk from the thickness of 10 μm to the thickness of 0.1 μm, and simultaneously a plurality of holes are formed therein. As a result, as shown in FIG. 6, a plurality of through regions 46 are formed in the upper electrode 42, and the peripheral portions 52 of the through regions 46 are turned into overhanging portions. In advance (of the sintering process), the film which will serve as the upper electrode 42 may be patterned by etching (wet etching or dry etching) or lift-off, and then may be sintered. In this case, recesses or slits may easily be formed as the through regions 46.

The emitter 40 may be covered with a suitable member, and then sintered such that the surface of the emitter 40 will not be exposed directly to the sintering atmosphere.

For using the electron emitter 12 as light-emitting device or a pixel of a display apparatus, as shown in FIG. 9, a transparent plate 60 made of glass or acrylic resin is placed above the upper electrode 42, and a collector electrode 62 in the form of a transparent electrode, for example, is placed on the reverse side of the transparent plate 60 (which faces the upper electrode 42), the collector

electrode 62 being coated with a phosphor 64. A bias voltage source 66 (collector voltage Vc) is connected to the collector electrode 62 through a resistor. The electron emitter 12 is naturally placed in a vacuum. The vacuum level in the atmosphere should preferably in the range from 10^{2} to 10^{-6} Pa and more preferably in the range from 10^{-3} to 10^{-5} Pa.

The reason for the above range is that in a lower vacuum, (1) many gas molecules would be present in the space, and a plasma can easily be generated and, if too an intensive plasma were generated, many positive ions thereof would impinge upon the upper electrode 42 and damage the same, and (2) emitted electrons would tend to impinge upon gas molecules prior to arrival at the collector electrode 62, failing to sufficiently excite the phosphor 64 with electrons that are sufficiently accelerated under the collector voltage Vc.

In a higher vacuum, though electrons would be liable to be emitted from a point where electric field concentrates, structural body supports and vacuum seals would be large in size, posing disadvantages on efforts to make the emitter smaller in size.

In the embodiment shown in FIG. 9, the collector electrode 62 is formed on the reverse side of the transparent plate 60, and the phosphor 64 is formed on the surface of the collector electrode 62 (which faces the upper electrode 42). According to another arrangement, as shown

in FIG. 10, the phosphor 64 may be formed on the reverse side of the transparent plate 60, and the collector electrode 62 may be formed in covering relation to the phosphor 64.

Such another arrangement is for use in a CRT or the like where the collector electrode 62 functions as a metal back. Electrons emitted from the emitter 40 pass through the collector electrode 62 into the phosphor 64, exciting the phosphor 64. Therefore, the collector electrode 62 is of a thickness which allows electrons to pass therethrough, preferably be 100 nm or less thick. As the kinetic energy of the emitted electrons is larger, the thickness of the collector electrode 62 may be increased.

This arrangement offers the following advantages:

(a) If the phosphor 64 is not electrically conductive, then the phosphor 64 is prevented from being charged (negatively), and an electric field for accelerating electrons can be maintained.

(b) The collector electrode 62 reflects light emitted from the phosphor 64, and discharges the light emitted from the phosphor 64 efficiently toward the transparent plate 60 (light emission surface).

(c) Electrons are prevented from impinging excessively upon the phosphor 64, thus preventing the phosphor 64 from being deteriorated and from producing a gas.

The principles of electron emission of the electron emitter 12 will be described below with reference to FIGS.

11A through 12C.

First, the electron emitter 12 emits electrons when a drive voltage is applied between the upper electrode 42 and the lower electrode 44. The drive voltage is defined as a voltage, such as a pulse voltage or an alternating-current voltage, which abruptly changed from a reference voltage (e.g., 0 V) or a voltage level that is higher or lower than the reference voltage to a voltage level that is lower or higher than the reference voltage.

A triple junction is formed in a region of contact between the upper surface of the emitter 40, the upper electrode 42, and a medium (e.g., a vacuum) around the electron emitter 12. The triple junction is defined as an electric field concentration region formed by a contact between the upper electrode 42, the emitter 40, and the vacuum. The triple junction includes a triple point where the upper electrode 42, the emitter 40, and the vacuum exist as one point.

With the arrangement of the electron emitter 12, the triple junction is formed on the overhanging portion 52 of the upper electrode 42 and the peripheral area of the upper electrode 42. Therefore, when the above drive voltage is applied between the upper electrode 42 and the lower electrode 44, an electric field concentration occurs at the triple junction.

In the description which follows, it is assumed that the emitter 40 is polarized in one direction, with dipoles

having negative poles facing toward the upper surface of the emitter 40 (see FIG. 11A).

At the point p1 (initial state) where the reference voltage (e.g., 0 V) is applied as shown in FIG. 5, since the negative poles of the dipole moments face toward the upper surface of the emitter 40, as shown in FIG. 11, almost no electrons are accumulated on the upper surface of the emitter 40.

Thereafter, when a negative voltage is applied and the level of the negative voltage is increased in the negative direction, the polarization starts being reversed substantially at the time the negative voltage exceeds a negative coercive voltage (see the point p2 in FIG. 5). All the polarization is reversed at the point p3 shown in FIG. 5 (see FIG. 1B). Because of the polarization reversal, an electric field concentration occurs at the triple junction, causing electrons to be accumulated in the portion of the emitter 40 which is exposed through the through region 46 of the upper electrode 42 and the portion of the emitter 40 which is near the peripheral portion of the upper electrode 42 (see FIG. 11C). In particular, electrons are emitted (emitted inwardly) from the upper electrode 42 toward the portion of the emitter 40 which is exposed through the through region 46 of the upper electrode 42. At the point p3 shown in FIG. 5, the accumulation of electrons is saturated.

Thereafter, when the level of the negative voltage is

reduced and a positive voltage is applied in excess of the reference voltage, the upper surface of the emitter 40 is kept charged up to a certain voltage level (see FIG. 12A). As the level of the positive voltage is increased, there is produced a region where the negative poles of dipole moments start facing the upper surface of the emitter 40 (see FIG. 12B) immediately prior to the point p4 in FIG. 5. When the level is further increased, electrons start being emitted after the point p4 in FIG. 5 (see FIG. 12C). When the positive voltage is increased in the positive direction, the amount of emitted electrons is increased. Substantially at the time the positive voltage exceeds the positive coercive voltage (the point p5), a region where the polarization is reversed again is increased. At the point p6, almost all the accumulated electrons are emitted, and the amount of polarization at this time is essentially the same as the amount of polarization in the initial state.

The characteristics of the electron emitter 12 has have the following features:

(A) If the negative coercive voltage is represented by v1 and the positive coercive voltage by v2, then

$|v1| < |v2|$

(B) More specifically, $1.5 \times |v1| < |v2|$

(C) If the rate of change of the polarization at the time the negative coercive voltage v1 is applied is represented by $\Delta q1/\Delta v1$ and the rate of change of the amount of positive charges and the rate of change of the

polarization at the time the positive coercive voltage v2 is applied is represented by $\Delta q2/\Delta v2$, then

$$(\Delta q1/\Delta v1) > (\Delta q2/\Delta v2)$$

(4) If the voltage at which the accumulation of electrons is saturated is represented by v3 and the voltage at which electrons start being emitted by v4, then

$$1 \le |v4|/|v3| \le 1.5$$

It can thus be seen that the electron emitter 12 has substantially the same characteristics as the features (1) through (4) of the characteristics of the electron emitter as described above.

Changes of the characteristics at the time the level of the negative voltage for the accumulation of electrons will be reviewed in relation to the three examples of amplitude modulation on the pulse signal Sp shown in FIGS. 2A through 2C and the three examples of pulse width modulation on the pulse signal Spa shown in FIGS. 4A through 4C. At the level Vsl of the negative voltage shown in FIGS. 2A and 4A, the amount of electrons accumulated in the electron emitter 12 is small as shown in FIG. 13A. At the level Vsm of the negative voltage shown in FIGS. 2B and 4B, the amount of electrons accumulated in the electron emitter 12 is medium as shown in FIG. 13B. At the level Vsh of the negative voltage shown in FIGS. 2C and 4C, the amount of electrons accumulated in the electron emitter 12 is large and is substantially saturated as shown in FIG. 13C.

However, as shown in FIGS. 13A through 13C, the voltage

level at the point p4 where electrons start being emitted is substantially the same. That is, even if the applied voltage changes to the voltage level indicated at the point p4 after electrons are accumulated, the amount of accumulated electrons does not change essentially. It can thus be seen that a memory effect has been caused.

Four experimental examples (first through fourth experimental examples) of the electron emitter 2 according to the present embodiment will be shown.

According to the first experimental example, the emission of electrons from the electron emitter 12 was observed. Specifically, as shown in FIG. 14A, a write pulse Pw having a voltage of - 70 V was applied to the electron emitter 12 to cause the electron emitter 12 to accumulate electrons, and thereafter a turn-on pulse Ph having a voltage of 280 V was applied to cause the electron emitter 12 to emit electrons. The emission of electrons was measured by detecting the light emission from the phosphor 64 with a light-detecting device (photodiode). The detected waveform is shown in FIG. 14B. The write pulse Pw and the turn-on pulse Ph had a duty cycle of 50 %.

It can be seen from the first experimental example that light starts to be emitted on a positive-going edge of the turn-on pulse Ph and the light emission is finished in an initial stage of the turn-on pulse Ph. Therefore, it is considered that the light emission will not be affected by shortening the period of the turn-on pulse Ph. This period

shortening will lead to a reduction in the period in which to apply the high voltage, resulting in a reduction in power consumption.

According to the second experimental example, how the amount of electrons emitted from the electron emitter 12 is changed by the amplitude of the write pulse Pw shown in FIG. 15 was observed. Changes in the amount of emitted electrons were measured by detecting the light emission from the phosphor 64 with a light-detecting device (photodiode), as with the first experimental example. The experimental results are shown in FIG. 16.

In FIG. 16, the solid-line curve A represents the characteristics at the time the turn-on pulse Ph had an amplitude of 200 V and the write pulse Pw had an amplitude changing from - 10 V to - 80 V, and the solid-line curve B represents the characteristics at the time the turn-on pulse Ph had an amplitude of 350 V and the write pulse Pw had an amplitude changing from - 10 V to - 80 V.

As illustrated in FIG. 16, when the write pulse Pw is changed from - 20 V to - 40 V, it can be understood that the light emission luminance changes substantially linearly. A comparison between the amplitudes 350 V and 200 V of the turn-on pulse Ph in particular indicates that a change in the light emission luminance in response to the write pulse Pw at the time the amplitude of the turn-on pulse Ph is 350 V has a wider dynamic range, which is advantageous for increased luminance and contrast for the display of images.

This tendency appears to be more advantageous as the amplitude of the turn-on pulse Ph increases in a range until the light emission luminance is saturated with respect to the setting of the amplitude of the turn-on pulse Ph. It is preferable to set the amplitude of the turn-on pulse Ph to an optimum value in relation to the withstand voltage and power consumption of the signal transmission system.

According to the third experimental example, how the amount of electrons emitted from the electron emitter 12 is changed by the amplitude of the turn-on pulse Ph shown in FIG. 15 was observed. Changes in the amount of emitted electrons were measured by detecting the light emission from the phosphor 64 with a light-detecting device (photodiode), as with the first experimental example. The experimental results are shown in FIG. 17.

In FIG. 17, the solid-line curve C represents the characteristics at the time the write pulse Pw had an amplitude of - 40 V and the turn-on pulse Ph had an amplitude changing from 50 V to 400 V, and the solid-line curve D represents the characteristics at the time the write pulse Pw had an amplitude of - 70 V and the turn-on pulse Ph had an amplitude changing from 50 V to 400 V.

As illustrated in FIG. 17, when the turn-on pulse Ph is changed from 100 V to 300 V, it can be understood that the light emission luminance changes substantially linearly. A comparison between the amplitudes -40 V and - 70 V of the write pulse Pw in particular indicates that a change in the

light emission luminance in response to the turn-on pulse Ph at the time the amplitude of the write pulse Pw is - 70 V has a wider dynamic range, which is advantageous for increased luminance and contrast for the display of images. This tendency appears to be more advantageous as the amplitude of the write pulse Pw increases in a range until the light emission luminance is saturated with respect to the setting of the amplitude of the write pulse Pw. It is preferable also in this case to set the amplitude (absolute value) of the write pulse Pw to an optimum value in relation to the withstand voltage and power consumption of the signal transmission system.

According to the fourth experimental example, how the amount of electrons emitted from the electron emitter 12 is changed by the level of the collector voltage Vc shown in FIG. 9 or 10 was observed. Changes in the amount of emitted electrons were measured by detecting the light emission from the phosphor 64 with a light-detecting device (photodiode), as with the first experimental example. The experimental results are shown in FIG. 18.

In FIG. 18, the solid-line curve E represents the characteristics at the time the level of the collector voltage Vc was 3 kV and the amplitude of the turn-on pulse Ph was changed from 80 V to 500 V, and the solid-line curve F represents the characteristics at the time the level of the collector voltage Vc was 7 kV and the amplitude of the turn-on pulse Ph was changed from 80 V to 500 V.

As illustrated in FIG. 18, it can be understood that a change in the light emission luminance in response to the turn-on pulse Ph has a wider dynamic range when the collector voltage Vc is 7 kV than when the collector voltage Vc is 3 kV, which is advantageous for increased luminance and contrast for the display of images. This tendency appears to be more advantageous as the level of the collector voltage Vc increases. It is preferable also in this case to set the level of the collector voltage Vc to an optimum value in relation to the withstand voltage and power consumption of the signal transmission system.

The electron emitter 12 also offers the following advantages: Since the upper electrode 42 has the plural through regions 46, electrons are uniformly emitted from each of the through regions 46 and the outer peripheral portions of the upper electrode 42. Thus, any variations in the overall electron emission characteristics of the electron emitter 12 are reduced, making it possible to facilitate the control of the electron emission and increase the electron emission efficiency.

Because the gap 54 is formed between the overhanging portion of the upper electrode 42 and the emitter 40, when the drive voltage is applied, an electric field concentration tends to be produced in the region of the gap 54. This leads to a higher efficiency of the electron emission, making the drive voltage lower (emitting electrons at a lower voltage level).

As described above, since the upper electrode 42 has the overhanging portion 52 on the peripheral portion of the through hole 46, together with the increased electric field concentration in the region of the gap 54, electrons are easily emitted from the overhanging portion 52 of the upper electrode 42. This leads to a higher output and higher efficiency of the electron emission, making the drive voltage lower. As the overhanging portion 52 of the upper electrode 42 functions as a gate electrode (a control electrode, a focusing electronic lens, or the like), the linearity of emitted electrons can be increased. This is effective in reducing crosstalk if a number of electron emitters 12 are arrayed for use as an electron source of the display apparatus 10.

As described above, the electron emitter 12 is capable of easily developing a high electric field concentration, provides many electron emission regions, has a higher output and higher efficiency of the electron emission, and can be driven at a lower voltage (lower power consumption).

With the electron emitter 12 in particular, at least the upper surface of the emitter 40 has the surface irregularities 48 due to the grain boundary of the dielectric material. As the upper electrode 42 has the through regions 46 in portions corresponding to the concavities 50 of the grain boundary of the dielectric material, the overhanging portions 52 of the upper electrode 42 can easily be realized.

The maximum angle θ between the upper surface of the emitter 40, i.e., the surface of the convexity 56 (which is also the inner wall surface of the concavity 50) of the grain boundary of the dielectric material, and the lower surface 56a of the overhanging portion 52 of the upper electrode 42 is in the range of $1° \leq \theta \leq 60°$. The maximum distance d in the vertical direction between the surface of the convexity 56 (the inner wall surface of the concavity 50) of the grain boundary of the dielectric material and the lower surface 56a of the overhanging portion 52 of the upper electrode 42 is in the range of $0\ \mu m < d \leq 10\ \mu m$. These arrangements make it possible to increase the degree of the electric field concentration in the region of the gap 54, resulting in a higher output and higher efficiency of the electron emission and making the drive voltage lower efficiently.

With the electron emitter 12, the through region 46 is in the shape of the hole 58. As shown in FIG. 7, the portions of the emitter 40 where the polarization is reversed or changed depending on the drive voltage applied between the upper electrode 42 and the lower electrode 44 (see FIG. 6) include a portion (first portion) 70 directly below the upper electrode 42 and a portion (second portion) 72 corresponding to a region extending from the inner peripheral edge of the through region 46 inwardly of the through region 46. Particularly, the second portion 72 changes depending on the level of the drive voltage and the

degree of the electric field concentration. With the electron emitter 12, the average diameter of the hole 58 is in the range from 0.1 μm to 10 μm. Insofar as the average diameter of the hole 58 is in this range, the distribution of electrons emitted through the through region 46 is almost free of any variations, allowing electrons to be emitted efficiently.

If the average diameter of the hole 58 is less than 0.1 μm, then the region where electrons are accumulated is made narrower, reducing the amount of emitted electrons. While one solution would be to form many holes 58, it would be difficult and highly costly to form many holes 58. If the average diameter of the hole 58 is in excess of 10 μm, then the proportion (share) of the portion (second portion) 72 which contributes the emission of electrons in the portion of the emitter 40 that is exposed through the through region 46 is reduced, resulting in a reduction in the electron emission efficiency.

The overhanging portion 52 of the upper electrode 42 may have upper and lower surfaces extending horizontally as shown in FIG. 7. Alternatively, as shown in FIG. 19, the overhanging portion 52 may have a lower surface 52a extending substantially horizontally and an upper end raised upwardly. Alternatively, as shown in FIG. 20, the overhanging portion 52 may have a lower surface 52a inclined progressively upwardly toward the center of the through hole 46. Further alternatively, as shown in FIG. 21, the

overhanging portion 52 may have a lower surface 52a inclined progressively downwardly toward the center of the through hole 46. The arrangement shown in FIG. 19 is capable of increasing the function as a gate electrode. The arrangement shown in FIG. 21 makes it easier to produce a higher electric field concentration for a higher output and higher efficiency of the electron emission because the gap 54 is narrower.

As shown in FIG. 21, the electron emitter 12 has in its electrical operation a capacitor C1 due to the emitter 40 and a cluster of capacitors Ca due to respective gaps 54, disposed between the upper electrode 42 and the lower electrode 44. The capacitors Ca due to the respective gaps 54 are connected parallel to each other into a single capacitor C2. In terms of an equivalent circuit, the capacitor C1 due to the emitter 40 is connected in series to the capacitor C2 which comprises the cluster of capacitors Ca.

Actually, the capacitor C1 due to the emitter 40 is not directly connected in series to the capacitor C2 which comprises the cluster of capacitors Ca, but the capacitive component that is connected in series varies depending on the number of the through regions 46 formed in the upper electrode 42 and the overall area of the through regions 46.

Capacitance calculations will be performed on the assumption that 25 % of the capacitor C1 due to the emitter 40 is connected in series to the capacitor C2 which

comprises the cluster of capacitors Ca, as shown in FIG. 23. Since the gaps 54 are in vacuum, the relative permittivity thereof is 1. It is assumed that the maximum distance d of the gaps 54 is 0.1 μm, the area S of each gap 54 is S = 1 μm × 1 μm, and the number of the gaps 54 is 10,000. It is also assumed that the emitter 40 has a relative permittivity of 2000, the emitter 40 has a thickness of 20 μm, and the confronting area of the upper and lower electrodes 42, 44 is 200 μm × 200 μm. The capacitor C2 which comprises the cluster of capacitors Ca has a capacitance of 0.885 pF, and the capacitor C1 due to the emitter 40 has a capacitance of 35.4 pF. If the portion of the capacitor C1 due to the emitter 40 which is connected in series to the capacitor C2 which comprises the cluster of capacitors Ca is 25 % of the entire capacitor C1, then that series-connected portion has a capacitance (including the capacitance of capacitor C2 which comprises the cluster of capacitors Ca) of 0.805 pF, and the remaining portion has a capacitance of 26.6 pF.

Because the series-connected portion and the remaining portion are connected parallel to each other, the overall capacitance is 27.5 pF. This capacitance is 78 % of the capacitance 35.4 pF of the capacitor C1 due to the emitter 40. Therefore, the overall capacitance is smaller than the capacitance of the capacitor C1 due to the emitter 40.

Consequently, the capacitance of the cluster of capacitors Ca due to the gaps 54 is relatively small. Because of the voltage division between the cluster of

capacitors Ca and the capacitor C1 due to the emitter 40, almost the entire voltage Va is applied across the gaps 54, which are effective to produce a higher output of the electron emission.

Since the capacitor C2 which comprises the cluster of capacitors Ca is connected in series to the capacitor C1 due to the emitter 40, the overall capacitance is smaller than the capacitance of the capacitor C1 due to the emitter 40. This is effective to provide such preferred characteristics that the electron emission is performed for a higher output and the overall power consumption is lower.

Three modifications of the electron emitter 12 will be described below with reference to FIGS. 24 through 26.

As shown in FIG. 24, an electron emitter 12a according to a first modification differs from the above electron emitter 12 in that the through region 46 has a shape, particularly a shape viewed from above, in the form of a recess 74. As shown in FIG. 24, the recess 74 should preferably be shaped such that a number of recesses 74 are successively formed into a saw-toothed recess 76. The saw-toothed recess 76 is effective to reduce variations in the distribution of electrons emitted through the through region 46 for efficient electron emission. Particularly, it is preferable to have the average width of the recesses 74 in the range from 0.1 μm to 10 μm. The average width represents the average of the lengths of a plurality of different line segments extending perpendicularly across the

central line of the recess 74.

As shown in FIG. 25, an electron emitter 12a according to a second modification differs from the above electron emitter 12 in that the through region 46 has a shape, particularly a shape viewed from above, in the form of a slit 78. The slit 78 is defined as something having a major axis (extending in a longitudinal direction) whose length is 10 times or more the length of the minor axis (extending in a transverse direction) thereof. Those having a major axis (extending in a longitudinal direction) whose length is less than 10 times the length of the minor axis (extending in a transverse direction) thereof are defined as holes 58 (see FIG. 8). The slit 78 includes a succession of holes 58 in communication with each other. The slit 78 should preferably have an average width ranging from 0.1 µm to 10 µm for reducing variations in the distribution of electrons emitted through the through region 46 for efficient electron emission. The average width represents the average of the lengths of a plurality of different line segments extending perpendicularly across the central line of the slit 78.

As shown in FIG. 26, an electron emitter 12c according to a third modification differs from the above electron emitter 12 in that a floating electrode 79 exists on the portion of the upper surface of the emitter 40 which corresponds to the through region 46, e.g., in the concavity 50 due to the grain boundary of the dielectric material. With this arrangement, in the state shown in FIG. 11C, the

floating electrode 79 forms a false lower electrode for promoting the emission (inward emission) of electrons from the upper electrode 42.

Various drive methods for the display apparatus 10 according to the present embodiment will be described below with reference to FIGS. 27 through 45. In the description of those drive methods, the electron emitter 12 shown in FIG. 6 is used.

A first drive method will first be described below with reference to FIGS. 27 and 28. FIG. 27 shows operation of pixels in the first row and the first column, the second row and the first column, and the nth row and the first column. The electron emitter 12 used in the first drive method has such characteristics that the coercive voltage v1 at the point p2 shown in FIG. 5 is - 20 V, for example, the coercive voltage v2 at the point p5 is + 70 V, the voltage v3 at the point p3 is - 50 V, and the voltage v4 at the point p4 is + 50 V.

As shown in FIG. 27, if the period in which to display one image is defined as one frame, then one charge accumulation period Td and one light emission period Th are included in one frame, and n selection periods Ts are included in one charge accumulation period Td. Since each selection period Ts becomes a selection period Ts for a corresponding row, it becomes a non-selection period Tn for non-corresponding n-1 rows.

According to the first drive method, all the electron

emitters 12 are scanned in the charge accumulation period Td, and voltages depending on the luminance levels of corresponding pixels are applied to a plurality of electron emitters 12 which correspond to pixels to be turned on (to emit light), thereby accumulating charges (electrons) in amounts depending on the luminance levels of the corresponding pixels in the electron emitters 12 which correspond to the pixels to be turned on. In the next light emission period Th, a constant voltage is applied to all the electron emitters 12 to cause the electron emitters 12 which correspond to the pixels to be turned on to emit electrons in amounts depending on the luminance levels of the corresponding pixels, thereby emitting light from the pixels to be turned on.

More specifically, as shown in FIG. 28, in the selection period Ts for the first row, a selection signal Ss of 50 V, for example, is supplied to the row selection line 18 of the first row, and a non-selection signal Sn of 0 V, for example, is applied to the row selection lines 18 of the other rows. A pixel signal Sd supplied to the signal lines 20 of the pixels to be turned on (to emit light) of all the pixels of the first row has a voltage in the range from 0 V to 30 V, depending on the luminance levels of the corresponding pixels. If the luminance level is maximum, then the voltage of the pixel signal Sd is 0 V. The pixel signal Sd is modulated depending on the luminance level by the amplitude modulating circuit 34 shown in FIG. 1 or the

pulse width modulating circuit 38 shown in FIG. 3.

Thus, a voltage ranging from - 50 V to - 20 V depending on the luminance level is applied between the upper and lower electrodes 42, 44 of the electron emitter 12 which corresponds to each of the pixels to be turned on in the first row. As a result, each electron emitter 12 accumulates electrons depending on the applied voltage. For example, the electron emitter 12 corresponding to the pixel in the first row and the first column is in a state at the point p3 shown in FIG. 5 as the luminance level of the pixel is maximum, and the portion of the emitter 40 which is exposed through the through region 46 of the upper electrode 42 accumulates a maximum amount of electrons.

A pixel signal Sd supplied to the electron emitters 12 which correspond to pixels to be turned off (to extinguish light) has a voltage of 50 V, for example. Therefore, a voltage of 0 V is applied to the electron emitters 12 which correspond to pixels to be turned off, bringing those electron emitters 12 into a state at the point p1 shown in FIG. 5, so that no electrons are accumulated in those electron emitters 12.

After the supply of the pixel signal Sd to the first row is finished, in the selection period Ts for the second row, a selection signal Ss of 50 V is supplied to the row selection line 18 of the second row, and a non-selection signal Sn of 0 V is applied to the row selection lines 18 of the other rows. In this case, a voltage ranging from - 50 V

to - 20 V depending on the luminance level is also applied between the upper and lower electrodes 42, 44 of the electron emitter 12 which corresponds to each of the pixels to be turned on. At this time, a voltage ranging from 0 V to 50 V is applied between the upper and lower electrodes 42, 44 of the electron emitter 12 which corresponds to each of unselected pixels in the first row, for example. Since this voltage is of a level not reaching the point 4 in FIG. 5, no electrons are emitted from the electron emitters 12 which correspond to the pixels to be turned on in the first row. That is, the unselected pixels in the first row are not affected by the pixel signal that is supplied to the selected pixels in the second row.

Similarly, in the selection period Ts for the nth row, a selection signal Ss of 50 V is supplied to the row selection line 18 of the nth row, and a non-selection signal Sn of 0 V is applied to the row selection lines 18 of the other rows. In this case, a voltage ranging from - 50 V to - 20 V depending on the luminance level is also applied between the upper and lower electrodes 42, 44 of the electron emitter 12 which corresponds to each of the pixels to be turned on. At this time, a voltage ranging from 0 V to 50 V is applied between the upper and lower electrodes 42, 44 of the electron emitter 12 which corresponds to each of unselected pixels in the first through (n-1)th rows. However, no electrons are emitted from the electron emitters 12 which correspond to the pixels to be turned on, of those

unselected pixels.

After elapse of the selection period Ts for the nth row, it is followed by the light emission period Th. In the light emission period Th, a reference voltage (e.g., 0 V) is applied from the signal supplying circuit 24 to the upper electrodes 42 of all the electron emitters 12, and a voltage of - 350 V (the sum of the voltage of - 400 V from the pulse power supply 30 and the power supply voltage 50 V from the row selecting circuit 22) is applied to the lower electrodes 44 of all the electron emitters 12. Thus, a high voltage (+ 350 V) is applied between the upper and lower electrodes 42, 44 of all the electron emitters 12. All the electron emitters 12 are now brought into a state at the point p6 shown in FIG. 5. As shown in FIG. 12C, electrons are emitted from the portion of the emitter 40 where the electrons have been accumulated, through the through region 46. Electrons are also emitted from near the outer peripheral portion of the upper electrode 42.

Electrons are thus emitted from the electron emitters 12 which correspond to the pixels to be turned on, and the emitted electrons are led to the collector electrodes 62 which correspond to those electron emitters 12, exciting the corresponding phosphors 64 which emit light. In this manner, an image is displayed on the surface of the transparent plate 60.

Subsequently, electrons are accumulated in the electron emitters 12 which correspond to the pixels to be turned on

(to emit light) in the charge accumulation period Td, and the accumulated electrons are emitted for fluorescent light emission in the light emission period Th, for thereby displaying a moving image or a still image on the surface of the transparent plate 60.

A second drive method will be described below with reference to FIGS. 29 through 31. According to the second drive method, as shown in FIG. 29, one frame is divided into a plurality of periods referred to as subfields SF1, SF2, ···, SFm, respectively, each including one charge accumulation period Td and one light emission period Th. The subfields SF1, SF2, ···, SFm have the same time intervals.

The luminance level assigned to the first subfield (the subfield SF1) is highest, and is progressively lowered as the subfields elapse successively.

According to the second drive method, all the electron emitters 12 are scanned in the charge accumulation period Td, and a constant voltage is applied to electron emitters 12 to be turned on, thereby accumulating a constant amount of charges in the electron emitters 12 to be turned on. In the next light emission period Th, voltages depending on the luminance levels assigned to the subfield (the subfield being currently scanned) are applied to all the electron emitters 12 to cause a plurality of electron emitters 12 which correspond to the pixels to be turned on to emit electrons in amounts depending on the luminance levels

assigned to the subfield, thereby emitting light from the pixels to be turned on. The second drive method employs a combination of the pulse number modulating process and the amplitude modulating process (the amplitude modulation of the voltage in the light emission period Th).

The second drive method employs a signal supplying circuit 80 shown in FIG. 30. A pulse power supply 82 is connected between a negative line between the signal supplying circuit 80 and the power supply circuit 28, and GND (ground). The pulse power supply 82 outputs a pulsed voltage waveform having a voltage of 0 V, for example, during the charge accumulation period Td, and a voltage of -330 V, for example, during the light emission period Th.

A pulse generating circuit 84 generates and outputs a pulse signal Sp1 having a constant pulse period and a constant amplitude (e.g., 50 V) during the charge accumulation period Td, and also generates and outputs a pulse signal Sp2 having a constant pulse period and a constant amplitude (e.g., - 280 V) during the light emission period Th.

As shown in FIG. 31, in the charge accumulation period Td, an amplitude modulating circuit 86 is controlled by the signal control circuit 26 to amplitude-modulate the voltage of the pulse signal Sp1 to be applied to the pixels to be turned on of the selected pixels into 0 V, for example, amplitude-modulate the voltage of the pulse signal Sp1 to be applied to the pixels to be turned off of the selected

pixels into 50 V, for example, and output the signals as the pixel signal Sd.

Therefore, as shown in FIG. 29, a voltage of - 50 V is applied to the electron emitters 12 which correspond to the pixels to be turned on of the selected pixels, and a voltage of 0 V is applied to the electron emitters 12 which correspond to the pixels to be turned off. A voltage of 0 V or 50 V is applied to the electron emitters 12 which correspond to the unselected pixels.

In the light emission period Th, the amplitude modulating circuit 86 is controlled by the signal control circuit 26 to amplitude-modulate the voltage into a voltage depending on the luminance level in the present subfield. In this example, as shown in FIG. 31, the voltage is amplitude-modulated in the range from - 280 V to 0 V. For example, in the light emission period Th of the first subfield SF1, the amplitude modulating circuit 86 applies a voltage of 0 V through the signal lines 20 to the upper electrodes 42 of all the electron emitters 12. In the light emission period Th of the second subfield SF2, the amplitude modulating circuit 86 applies a voltage of - 175 V to the upper electrodes 42 of all the electron emitters 12. In the light emission period Th of the mth subfield SFm, the amplitude modulating circuit 86 applies a voltage of - 280 V to the upper electrodes 42 of all the electron emitters 12. In the light emission periods Th of the subfields SF1, SF2, ···, SFm, the row selecting circuit 22 applies a voltage of

- 350 V through all the row select lines 18 to the lower electrodes 44 of all the electron emitters 12.

Accordingly, as shown in FIG. 29, in the light emission period Th of the first subfield SF1, a voltage of 350 V is applied to all the electron emitters 12. In the light emission period Th of the second subfield SF2, a voltage of 175 V is applied to all the electron emitters 12. In the light emission period Th of the mth subfield SFm, a voltage of 70 V is applied to all the electron emitters 12.

Specifically, only the first subfield SF1 and the second subfield SF2 will be considered below with reference to FIG. 29. If the luminance level of the first subfield SF1 is 64, for example, and the luminance level of the second subfield SF2 is 32, the pixel in the first row and the first column has a luminance level of 64 because the first subfield SF1 is turned on and the second subfield SF2 is turned off. The pixel in the second row and the first column has a luminance level of 64 + 32 = 96 because the first subfield SF1 is turned on and the second subfield SF2 is turned on. Similarly, the pixel in the nth row and the first column has a luminance level of 32 because the first subfield SF1 is turned off and the second subfield SF2 is turned on.

In this manner, in each subfield, a constant amount of electrons are accumulated in the electron emitters 12 which correspond to the pixels to be turned on (to emit light) in the charge accumulation period Td, and a voltage depending

on the luminance level of the subfield is applied to emit the accumulated electrons for fluorescent light emission in the light emission period Th, for thereby displaying a moving image or a still image on the surface of the transparent plate 60.

A third drive method will be described below with reference to FIGS. 32 and 33. According to the third drive method, as shown in FIG. 32, the concept of subfields is employed as with the second drive method. The subfields SF1, SF2, ···, SFm have the same time intervals. The luminance level assigned to the first subfield (the subfield SF1) is highest, and is progressively lowered as the subfields elapse successively.

According to the third drive method, all the electron emitters 12 are scanned in the charge accumulation period Td, and voltages depending on the luminance levels assigned to a subfield are applied to electron emitters 12 to be turned on, thereby accumulating charges in amounts depending on the luminance levels assigned to the subfield in the electron emitters 12 to be turned on. In the next light emission period Th, a constant voltage is applied to all the electron emitters 12 to cause the electron emitters 12 which correspond to the pixels to be turned on to emit electrons in amounts depending on the luminance levels assigned to the subfield, thereby emitting light from the pixels to be turned on. The third drive method employs a combination of the pulse number modulating process and the amplitude

modulating process (the amplitude modulation of the voltage in the charge accumulation period) or a combination of the pulse number modulating process and the pulse width modulating process (the pulse width modulation of the voltage in the charge accumulation period).

The third drive method employs the signal supplying circuit 24, 24a shown in FIG. 1 or 3. If the amplitude modulating circuit 34 shown in FIG. 1, for example, is employed, then in the charge accumulation period Td, the amplitude modulating circuit 34 is controlled by the signal control circuit 26 to amplitude-modulate the voltage of the pulse signal Sp to be applied to the pixels to be turned on of the selected pixels into a voltage depending on the luminance level of the present subfield, and outputs the modulated voltage as the pixel signal Sd. In this example, the voltage is amplitude-modulated in a range from 0 V to 30 V.

Accordingly, as shown in FIG. 32, in the charge accumulation period Td of the first subfield SF1, a voltage of 0 V is applied to the upper electrodes 42 of the electron emitters 12 which correspond to the pixels to be turned on when all the electron emitters 12 are scanned. In the charge accumulation period Td of the second subfield SF2, a voltage of 15 V is applied to the upper electrodes 42 of the electron emitters 12 which correspond to the pixels to be turned on. In the charge accumulation period Td of the mth subfield SFm, a voltage of 30 V is applied to the upper

electrodes 42 of the electron emitters 12 which correspond to the pixels to be turned on.

Therefore, as shown in FIG. 32, in the charge accumulation period Td of the first subfield SF1, a voltage of - 50 V is applied to the electron emitters 12 which correspond to the pixels to be turned on. In the charge accumulation period Td of the second subfield SF2, a voltage of - 35 V is applied to the electron emitters 12 which correspond to the pixels to be turned on. In the charge accumulation period Td of the mth subfield SFm, a voltage of - 20 V is applied to the electron emitters 12 which correspond to the pixels to be turned on.

In the light emission periods Th of the subfields SF1, SF2, ···, SFm, the amplitude modulating circuit 34 applies a voltage of 0 V through the signal lines 20 to the upper electrodes 42 of all the electron emitters 12, and the row selecting circuit 22 applies a voltage of - 350 V through all the row select lines 18 to the lower electrodes 44 of all the electron emitters 12. Thus, a voltage of 350 V is applied to all the electron emitters 12 in the light emission periods Th of the subfields SF1, SF2, ···, SFm.

In this manner, in each subfield, an amount of electrons depending on the luminance level of the subfield are accumulated in the electron emitters 12 which correspond to the pixels to be turned on (to emit light) in the charge accumulation period Td, and the accumulated electrons are emitted for fluorescent light emission in the light emission

period Th, for thereby displaying a moving image or a still image on the surface of the transparent plate 60.

A fourth drive method will be described below with reference to FIGS. 34 through 36. According to the fourth drive method, as shown in FIG. 34, one frame is divided into a plurality of periods, each having the same luminance level, referred to as linear subfields LSF1, LSF2, ···, LSFm, respectively, each including one charge accumulation period Td and one light emission period Th. The linear subfields LSF1, LSF2, ···, LSFm have the same time intervals.

According to the fourth drive method, all the electron emitters 12 are scanned in the charge accumulation period Td, and a constant voltage is applied to electron emitters 12 to be turned on in a linear subfield (a linear subfield being presently scanned), thereby accumulating a constant amount of charges in the electron emitters 12 to be turned on in the linear subfield. In the next light emission period Th, a constant voltage is applied to all the electron emitters 12 to cause a plurality of electron emitters 12 which correspond to the pixels to be turned on in the linear subfield to emit electrons in a constant amount, thereby emitting light from the pixels to be turned on. The fourth drive method employs the pulse number modulating process.

The fourth drive method employs a signal supplying circuit 90 shown in FIG. 35. A pulse power supply 92 is connected between a negative line between the signal

supplying circuit 90 and the power supply circuit 28, and GND (ground). The pulse power supply 92 outputs a pulsed voltage waveform having a voltage of 0 V, for example, during the charge accumulation period Td, and a voltage of - 200 V, for example, during the light emission period Th.

A pulse generating circuit 94 generates and outputs a pulse signal Sp3 having a constant pulse period and a constant amplitude (e.g., 50 V) during the charge accumulation period Td, and also generates and outputs a pulse signal Sp4 having a constant pulse period and a constant amplitude (e.g., - 150 V) during the light emission period Th.

As shown in FIG. 36, in the charge accumulation period Td, an amplitude modulating circuit 96 is controlled by the signal control circuit 26 to amplitude-modulate the voltage of the pulse signal Sp3 to be applied to the pixels to be turned on of the selected pixels into 0 V, for example, amplitude-modulate the voltage of the pulse signal Sp3 to be applied to the pixels to be turned off of the selected pixels into 50 V, for example, and output the signals as the pixel signal Sd.

Therefore, as shown in FIG. 34, a voltage of - 50 V is applied to the electron emitters 12 which correspond to the pixels to be turned on of the selected pixels, and a voltage of 0 V is applied to the electron emitters 12 which correspond to the pixels to be turned off. A voltage of 0 V or 50 V is applied to the electron emitters 12 which

correspond to the unselected pixels.

In the light emission periods Th of the linear subfields LSF1, LSF2, ···, LSFm, the amplitude modulating circuit 96 applies a voltage of - 150 V through the signal lines 20 to the upper electrodes 42 of all the electron emitters 12, and the row selecting circuit 22 applies a voltage of - 350 V through all the row select lines 18 to the lower electrodes 44 of all the electron emitters 12. In the light emission periods Th of the linear subfields LSF1, LSF2, ···, LSFm, therefore, a voltage of 200 V is applied to all the electron emitters 12. If the signal supplying circuit 90 is designed to apply a voltage of 350 V to all the electron emitters 12 in the light emission periods Th, then the signal supplying circuit 24 shown in FIG. 1 can be employed.

Each pixel is turned on in the charge accumulation periods Td of a succession of linear subfields LSF1, LSF2, ···, LSFm depending on the corresponding luminance level, and is turned off in the charge accumulation periods Td of the remaining linear subfields.

For example, as shown in FIG. 34, if the luminance level of the pixel in the first row and the first column is "64", then a voltage of - 50 V is applied to the electron emitter 12 which corresponds to the pixel in the charge accumulation periods Td of a number of successive linear subfields depending on the luminance level "64", causing the electron emitter 12 to emit light in the light emission

periods Th. If the luminance level of the pixel in the second row and the first column is "32", then a voltage of - 50 V is applied to the electron emitter 12 which corresponds to the pixel in the charge accumulation periods Td of a number of successive linear subfields depending on the luminance level "32" (which number is half the number corresponding to the luminance level "64"), causing the electron emitter 12 to emit light in the light emission periods Th. If the luminance level of the pixel in the nth row and the first column is "8", then a voltage of - 50 V is applied to the electron emitter 12 which corresponds to the pixel in the charge accumulation periods Td of a number of successive linear subfields depending on the luminance level "8" (which number is 1/8 of the number corresponding to the luminance level "64"), causing the electron emitter 12 to emit light in the light emission periods Th.

In this manner, in each linear subfield, a constant amount of electrons are accumulated in the electron emitters 12 which correspond to the pixels to be turned on (to emit light) in the charge accumulation period Td, and the accumulated electrons are emitted for fluorescent light emission in the light emission period Th, for thereby displaying a moving image or a still image on the surface of the transparent plate 60.

A fifth drive method will be described below with reference to FIGS. 37 through 39. According to the fifth drive method, one frame includes one charge accumulation

period Td and one light emission period Th, as with the first drive method.

In the description which follows, it is assumed that the electron emitter 12 has such characteristics that the coercive voltage v1 at the point p2 shown in FIG. 5 is - 20 V, for example, the coercive voltage v2 at the point p5 is + 140 V, the voltage v3 at the point p3 is - 70 V, and the voltage v4 at the point p4 is + 110 V.

According to the fifth drive method, in the charge accumulation period Td, a constant voltage is applied to all the electron emitters 12 to accumulate a constant amount of charges in all the electron emitters 12. In the next light emission period Th, all the electron emitters 12 are scanned, and voltages depending on the luminance levels of corresponding pixels to be turned on are applied to a plurality of electron emitters 12 which correspond to the pixels to be turned on, causing the electron emitters 12 which correspond to the pixels to be turned on to emit amounts of electrons depending on the luminance levels of the corresponding pixels thereby to emit light from the pixels to be turned on. The fifth drive method employs the amplitude modulating process (the amplitude modulation of the voltage in the light emission period Th).

The fifth drive method employs a row selecting circuit 100 and a signal supplying circuit 102 shown in FIG. 38. The row selecting circuit 100 is supplied with voltages of 100 V, 70 V, and 0 V, for example, from the power supply

circuit 28. The signal supplying circuit 102 is supplied with voltages of 200 V and 0 V, for example, from the power supply circuit 28.

As shown in FIG. 39, the row selecting circuit 100 outputs a constant voltage (e.g., 70 V) in the charge accumulating period Td. In the light emission period Th, the row selecting circuit 100 outputs a voltage of 0 V, for example, to the selected rows, and outputs a voltage of 100 V, for example, to the unselected rows.

A pulse generating circuit 104 of the signal supplying circuit 102 outputs a reference voltage (e.g., 0 V) during the charge accumulation period Td, and generates and outputs a pulse signal Sp5 having a constant period and a constant amplitude (e.g., 200 V) during the light emission period Th.

An amplitude modulating circuit 106 outputs the reference voltage from the pulse generating circuit 104 as it is in the charge accumulation period Td. In the light emission period Th, the amplitude modulating circuit 106 amplitude-modulates the voltage of the pulse signal Sp5 to be applied to the pixels to be turned on of the selected pixels in a range from 110 V to 200 V depending on the luminance levels of those pixels, amplitude-modulates the voltage of the pulse signal Sp5 be applied to the pixels to be turned off into a voltage of 100 V, for example, and outputs the signals as the pixel signal Sd.

In this manner, as shown in FIG. 37, in the charge accumulation period Td, a voltage of - 70 V is applied to

all the electron emitters 12 to accumulate a constant amount of charges (electrons) in all the electron emitters 12.

In the next light emission period Th, a voltage ranging from 110 V to 200 V depending on the luminance level is applied to the electron emitters 12 which correspond to the pixels to be turned on of the selected pixels, and a voltage of 100 V is applied to the electron emitters 12 which correspond to the pixels to be turned off, not shown. A voltage ranging from 10 V to 100 V is applied to the electron emitters 12 which correspond to the unselected pixels.

In the example shown in FIG. 37, a voltage of 200 V is applied to the electron emitter 12 which corresponds to the pixel in the first row and the first column to cause the electron emitter 12 to emit light at a luminance level of "64". A voltage of 150 V is applied to the electron emitter 12 which corresponds to the pixel in the second row and the first column to cause the electron emitter 12 to emit light at a luminance level of "32". A voltage of 170 V is applied to the electron emitter 12 which corresponds to the pixel in the nth row and the first column to cause the electron emitter 12 to emit light at a luminance level of "48". Though a voltage ranging from 10 V to 100 V is applied to the electron emitters 12 which correspond to the unselected pixels, since this voltage is of a level not reaching the point 4 (110 V in this example) in FIG. 5, no electrons are emitted from the electron emitters 12 which correspond to

the unselected pixels. That is, the unselected pixels are not affected by the pixel signal Sd that is supplied to the selected pixels.

In this manner, in each subfield, a constant amount of electrons are accumulated in the electron emitters 12 which correspond to the pixels to be turned on (to emit light) in the charge accumulation period Td, and voltages depending on the luminance levels of the pixels to be turned on are applied to emit the accumulated electrons for fluorescent light emission in the light emission period Th, for thereby displaying a moving image or a still image on the surface of the transparent plate 60.

A sixth drive method will be described below with reference to FIGS. 40 and 41. According to the sixth drive method, as shown in FIG. 40, the concept of subfields is employed as with the second drive method. The subfields SF1, SF2, ···, SFm have the same time intervals. The luminance level assigned to the first subfield (the subfield SF1) is highest, and is progressively lowered as the subfields elapse successively.

According to the sixth drive method, voltages depending on the luminance levels assigned to a subfield are applied to all the electron emitters 12, thereby accumulating charges in amounts depending on the luminance levels assigned to the subfield in all the electron emitters 12. In the next light emission period Th, all the electron emitters 12 are scanned, and a constant voltage is applied

to the electron emitters 12 to be turned on to cause the electron emitters 12 which correspond to the pixels to be turned on to emit electrons in amounts depending on the luminance levels assigned to the subfield, thereby emitting light from the pixels to be turned on. The sixth drive method employs a combination of the pulse number modulating process and the amplitude modulating process (the amplitude modulation of the voltage in the charge accumulation period Td) or a combination of the pulse number modulating process and the pulse width modulating process (the pulse width modulation of the voltage in the charge accumulation period Td).

The sixth drive method can employ the signal supplying circuit 102 shown in FIG. 38. In particular, the sixth drive method can employ the amplitude modulating circuit 34 shown in FIG. 1 or the pulse width modulating circuit 38 shown in FIG. 3. If the amplitude modulating circuit 34 shown in FIG. 1, for example, is employed, then in the charge accumulation period Td, the amplitude modulating circuit 34 is controlled by the signal control circuit 26 to amplitude-modulate the voltages of all the pulse signals Sp into a voltage depending on the luminance level of the present subfield, and output the modulated voltages as the pixel signal Sd. In this example, the voltages are amplitude-modulated in a range from 0 V to 50 V.

Accordingly, as shown in FIG. 40, in the charge accumulation period Td of the first subfield SF1, a voltage

of 0 V is applied to the upper electrodes 42 of all the electron emitters 12. In the charge accumulation period Td of the second subfield SF2, a voltage of 25 V is applied to the upper electrodes 42 of all the electron emitters 12. In the charge accumulation period Td of the mth subfield SFm, a voltage of 50 V is applied to the upper electrodes 42 of all the electron emitters 12.

Therefore, in the charge accumulation period Td of the first subfield SF1, a voltage of - 70 V is applied to all the electron emitters 12. In the charge accumulation period Td of the second subfield SF2, a voltage of - 45 V is applied to all the electron emitters 12. In the charge accumulation period Td of the mth subfield SFm, a voltage of - 20 V is applied to all the electron emitters 12.

In the light emission periods Th of the subfields SF1, SF2, ···, SFm, the amplitude modulating circuit 34 is controlled by the signal control circuit 26 to amplitude-modulate the voltage of the pulse signal Sp5 to be applied to the pixels to be turned on of the selected pixels into a voltage of 200 V, amplitude-modulate the voltage of the pulse signal Sp5 to be applied to the pixels to be turned off into a voltage of 100 V, and output the voltages as the pixel signal Sd.

Consequently, as shown in FIG. 41, the light emission periods Th of the subfields SF1, SF2, ···, SFm, a voltage of 200 V is applied to the electron emitters 12 which correspond to the pixels to be turned on, and a voltage of

100 V is applied to the electron emitters 12 which correspond to the pixels to be turned off. A voltage of 0 V or 100 V is applied to the electron emitters 12 which are not selected.

Specifically, only the first subfield SF1 and the second subfield SF2 will be considered below with reference to FIG. 40. If the luminance level of the first subfield SF1 is 64, for example, and the luminance level of the second subfield SF2 is 32, the pixel in the first row and the first column has a luminance level of 64 because the first subfield SF1 is turned on and the second subfield SF2 is turned off. The pixel in the second row and the first column has a luminance level of 64 + 32 = 96 because the first subfield SF1 is turned on and the second subfield SF2 is turned on. Similarly, the pixel in the nth row and the first column has a luminance level of 32 because the first subfield SF1 is turned off and the second subfield SF2 is turned on.

In this manner, in each subfield, electrons depending on the luminance level of the subfield are accumulated in all the electron emitters 12 in the charge accumulation period Td, and the accumulated electrons in the pixels to be turned on (to emit light) are emitted for fluorescent light emission in the light emission period Th, for thereby displaying a moving image or a still image on the surface of the transparent plate 60.

A seventh drive method will be described below with

reference to FIGS. 42 and 43. According to the seventh drive method, as shown in FIG. 42, the concept of subfields is employed as with the second drive method. The subfields SF1, SF2, ···, SFm have the same time intervals. The luminance level assigned to the first subfield (the subfield SF1) is highest, and is progressively lowered as the subfields elapse successively.

According to the seventh drive method, a constant voltage is applied to all the electron emitters 12, thereby accumulating a constant amount of charges in all the electron emitters 12. In the next light emission period Th, all the electron emitters 12 are scanned, and voltages depending on the luminance levels assigned to a subfield are applied to the electron emitters 12 to be turned on, causing to cause the electron emitters 12 which correspond to the pixels to be turned on to emit electrons in amounts depending on the luminance levels assigned to the subfield, thereby emitting light from the pixels to be turned on. The seventh drive method employs a combination of the pulse number modulating process and the amplitude modulating process (the amplitude modulation of the voltage in the charge accumulation period Td).

The seventh drive method can employ the signal supplying circuit 102 shown in FIG. 38. As shown in FIG. 43, the amplitude modulating circuit 106 is controlled by the signal control circuit 26 to output the reference voltage from the pulse generating circuit 104 as it is in

the charge accumulation period Td. In the light emission period Th, the amplitude modulating circuit 106 is controlled by the signal control circuit 26 to amplitude-modulate the voltage of the pulse signal Sp5 to be applied to the pixels to be turned on of the selected pixels in a range from 110 V to 200 V depending on the luminance level of the present subfield, amplitude-modulate the voltage of the pulse signal Sp5 be applied to the pixels to be turned off into a voltage of 100 V, for example, and output the signals as the pixel signal Sd.

Therefore, as shown in FIG. 42, in the charge accumulation period Td, a voltage of - 70 V is applied to all the electron emitters 12, accumulating a constant amount of charges (electrons) in all the electron emitters 12.

In the next light emission period Th, as shown in FIG. 43, a voltage ranging from 110 V to 200 V depending on the luminance levels of the present subfield is applied to the electron emitters 12 which correspond to the pixels to be turned on of the selected pixels, and a voltage of 100 V is applied to the electron emitters 12 which correspond to the pixels to be turned off. For example, as shown in FIG. 42, in the light emission period Th of the first subfield SF1, a voltage of 200 V is applied to the electron emitters 12 which correspond to the pixels to be turned on. In the light emission period Th of the second subfield SF2, a voltage of 155 V is applied to the electron emitters 12 which correspond to the pixels to be turned on. In the

light emission period Th of the mth subfield SFm, a voltage of 110 V is applied to the electron emitters 12 which correspond to the pixels to be turned on. A voltage ranging from 10 V to 100 V is applied to the electron emitters 12 which correspond to the unselected pixels.

In this manner, in each subfield, a constant amount of electrons are accumulated in the electron emitters 12 which correspond to the pixels to be turned on (to emit light) in the charge accumulation period Td, and voltages depending on the luminance levels of the subfield are applied to emit the accumulated electrons for fluorescent light emission in the light emission period Th, for thereby displaying a moving image or a still image on the surface of the transparent plate 60.

An eighth drive method will be described below with reference to FIGS. 44 and 45. According to the eighth drive method, as shown in FIG. 44, the concept of linear subfields is employed as with the fourth drive method. The linear subfields LSF1, LSF2, ···, LSFm have the same time intervals and luminance levels.

According to the eighth drive method, a constant voltage is applied to all the electron emitters 12 to accumulate a constant amount of charges in the electron emitters 12 to be turned on in a linear subfield in the charge accumulation period Td. In the next light emission period Th, all the electron emitters 12 are scanned, and a constant voltage is applied to the electron emitters 12 to

be turned on in the linear subfield, causing the electron emitters 12 which correspond the pixels to be turned on in the linear subfield to emit light thereby to emit light from the pixels to be turned on. The eighth drive method employs the pulse number modulating process.

The eighth drive method can employ the signal supplying circuit 102 shown in FIG. 38. The amplitude modulating circuit 106 is controlled by the signal control circuit 26 to output the reference voltage from the pulse generating circuit 104 as it is in the charge accumulation period Td. In the light emission period Th, the amplitude modulating circuit 106 is controlled by the signal control circuit 26 to amplitude-modulate the voltage of the pulse signal Sp5 to be applied to the pixels to be turned on of the selected pixels into a voltage of 200 V, for example, amplitude-modulate the voltage of the pulse signal Sp5 be applied to the pixels to be turned off into a voltage of 100 V, for example, and output the signals as the pixel signal Sd.

Therefore, as shown in FIG. 45, in the charge accumulation period Td, a voltage of - 70 V is applied to all the electron emitters 12, accumulating a constant amount of charges (electrons) in all the electron emitters 12.

In the next light emission period Th, as shown in FIG. 45, a voltage of 200 V is applied to the electron emitters 12 which correspond to the pixels to be turned on of the selected pixels, and a voltage of 100 V is applied to the electron emitters 12 which correspond to the pixels to be

turned off. A voltage ranging from 10 V to 100 V is applied to the electron emitters 12 which correspond to the unselected pixels.

Each pixel is turned on in the light emission periods Th of a succession of linear subfields LSF1, LSF2, ···, LSFm depending on the corresponding luminance level, and is turned off in the light emission period periods Th of the remaining linear subfields.

For example, as shown in FIG. 44, if the luminance level of the pixel in the first row and the first column is "64", then a voltage of 200 V is applied to the electron emitter 12 which corresponds to the pixel in the light emission periods Th of a number of successive linear subfields depending on the luminance level "64", causing the electron emitter 12 to emit light in the light emission periods Th. If the luminance level of the pixel in the second row and the first column is "32", then a voltage of 200 V is applied to the electron emitter 12 which corresponds to the pixel in the light emission period Th of a number of successive linear subfields depending on the luminance level "32", causing the electron emitter 12 to emit light in the light emission periods Th. If the luminance level of the pixel in the nth row and the first column is "8", then a voltage of 200 V is applied to the electron emitter 12 which corresponds to the pixel in the light emission periods Th of a number of successive linear subfields depending on the luminance level "8", causing the

electron emitter 12 to emit light in the light emission periods Th.

In this manner, in each linear subfield, a constant amount of electrons are accumulated in all the electron emitters 12 in the charge accumulation period Td, and a constant voltage is applied to the electron emitters 12 which correspond to the pixels to be turned on (to emit light) to emit the accumulated electrons for fluorescent light emission in the light emission period Th, for thereby displaying a moving image or a still image on the surface of the transparent plate 60.

In the display apparatus 10 according to the present embodiment, as described above, necessary charges are accumulated in all the electron emitters 12 in the charge accumulation period Td. In the subsequent light emission period Th, a voltage required to emit electrons is applied to all the electron emitters 12 to cause a plurality of electron emitters 12 which correspond to the pixels to be turned on to emit the electrons for thereby emitting light from the pixels to be turned on.

Usually, if pixels are made up of electron emitters 12, then a high voltage needs to be applied to the electron emitters 12 to emit light from the pixels. Therefore, for accumulating charges in the pixels and emitting light from the pixels when the pixels are scanned, a high voltage needs to be applied to the pixels during a period (e.g., one frame) for displaying one image, resulting in the problem of

increased electric power consumption. Circuits for selecting electron emitters 12 and supplying the pixel signals Sd to the selected electron emitters 12 need to be able to handle the high voltage.

According to the present embodiment, after charges have been accumulated in all the electron emitters 12, a voltage is applied to all the electron emitters 12, emitting light from the pixels which correspond to the electron emitters 12 to be turned on.

Therefore, the period Th during which a voltage (emission voltage) for emitting electrons is applied to all the electron emitters 12 is necessarily shorter than one frame. As can be seen from the first experimental example shown in FIGS. 14A and 14B, since the period during which to apply the emission voltage can be reduced, the power consumption can be made much smaller than if charges are accumulated and light is emitted when the pixels are scanned.

Because the period Td for accumulating charges in electron emitters 12 and the period Th for emitting electrons from electron emitters 12 which correspond to the pixels to be turned on are separated from each other, the circuit for applying voltages depending on luminance levels to the electron emitters 12 can be driven at a low voltage.

The pixel signal Sd depending on an image and the selection signal Ss/non-selection signal Sn in the charge accumulation period Td need to be applied for each row or

each column. As can be seen from the above embodiment, as the drive voltage may be of a few tens of volts, an inexpensive multi-output driver for use with fluorescent display tubes may be used. In the light emission period Th, a voltage for emitting sufficient electrons is likely to be higher than the drive voltage. Since all the pixels to be turned on may be driven altogether, no multi-output circuit component is required. For example, a one-output drive circuit in the form of a discrete component having a high withstand voltage may be sufficient. Therefore, the drive circuit may be inexpensive and may be small in circuit scale.

The display apparatus 10 according to the present embodiment can be used as electron beam irradiation apparatus, light sources, LED alternatives, electronic parts manufacturing apparatus, and electronic circuit components, in addition to display apparatus.

An electron beam in an electron beam irradiation apparatus has a higher energy and a better absorption capability than ultraviolet rays in ultraviolet ray irradiation apparatus that are presently in widespread use. The display apparatus may be used to solidify insulating films in superposing wafers for semiconductor devices, harden printing inks without irregularities for drying prints, and sterilize medical devices while being kept in packages.

The display apparatus may also be used as high-

luminance, high-efficiency light sources for use in projectors, for example, which may employ ultrahigh-pressure mercury lamps. The light source using the electron emitter according to the present embodiment is compact, has a long service life, has a fast response speed for light emission. The electron emitter does not use any mercury, and the electron emitter is environmentally friendly.

The display apparatus may also be used as LED alternatives in surface light sources such as indoor illumination units, automobile lamps, traffic signal devices, and also in chip light sources, traffic signal devices, and backlight units for small-size liquid-crystal display devices for cellular phones.

The display apparatus may also be used in electronic parts manufacturing apparatus as electron beam sources for film growing apparatus such as electron beam evaporation apparatus, electron sources for generating a plasma (to activate a gas or the like) in plasma CVD apparatus, and electron sources for decomposing gases. The display apparatus may also be used in vacuum micro devices including ultrahigh-speed devices operable in a tera-Hz range and large-current output devices. The display apparatus may also preferably be used as printer components, i.e., light emission devices for applying light to a photosensitive drum in combination with a phosphor, and electron sources for charging dielectric materials.

The display apparatus may also be used in electronic

circuit components including digital devices such as switches, relays, diodes, etc. and analog devices such as operational amplifiers, etc. as they can be designed for outputting large currents and higher amplification factors.

The pixels of the display apparatus 10 which have the collector electrode 62 coated with the phosphor 64 as shown in FIGS. 9 and 10 offer the following advantages:

(1) The display apparatus can be much thinner (the panel thickness = several mm) than CRTs.

(2) Since the display apparatus emits natural light from the phosphor 64, the display apparatus can provide a wide angle of view which is about 180° unlike LCDs (liquid crystal displays) and LEDs (light-emitting diodes).

(3) Since the display apparatus employs a surface electron source, it produces less image distortions than CRTs.

(4) The display apparatus can respond more quickly than LCDs, and can display moving images free of after image with a high-speed response on the order of μsec.

(5) The display apparatus consumes an electric power of about 100 W in terms of a 40-inch size, and hence is characterized by lower power consumption than CRTs, PDPs (plasma displays), LCDs, and LEDs.

(6) The display apparatus has a wider operating temperature range (- 40 to + 85°C) than PDPs and LCDs. LCDs have lower response speeds at lower temperatures.

(7) The display apparatus can produce higher luminance

than conventional FED displays as the fluorescent material can be excited by a large current output.

(8) The display apparatus can be driven at a lower voltage than conventional FED displays because the drive voltage can be controlled by the polarization reversing characteristics and film thickness of the piezoelectric material.

Because of the above various advantages, the display apparatus can be used in a variety of applications described below.

(1) Since the display apparatus can produce higher luminance and consume lower electric power, it is optimum for use as 30- through 60-inch displays for home use (television and home theaters) and public use (waiting rooms, karaoke rooms, etc.).

(2) Inasmuch as the display apparatus can produce higher luminance, can provide large screen sizes, can display full-color images, and can display high-definition images, it is optimum for use as horizontally or vertically long, specially shaped displays, displays in exhibitions, and message boards for information guides.

(3) Because the display apparatus can provide a wider angle of view due to higher luminance and fluorescent excitation, and can be operated in a wider operating temperature range due to vacuum modularization thereof, it is optimum for use as displays on vehicles. Displays for use on vehicles need to have a horizontally long 8-inch size

whose horizontal and vertical lengths have a ratio of 15 : 9 (pixel pitch = 0.14 mm), an operating temperature in the range from - 30 to + 85° C, and a luminance level ranging from 500 to 600 cd/m^2 in an oblique direction.

Because of the above various advantages, the display apparatus can be used as a variety of light sources described below.

(1) Since the display apparatus can produce higher luminance and consume lower electric power, it is optimum for use as projector light sources which are required to have a luminance level of 2000 lumens.

(2) Because the display apparatus can easily provide a high-luminance two-dimensional array light source, can be operated in a wide temperature range, and have their light emission efficiency unchanged in outdoor environments, it is promising as an alternative of LEDs. For example, the display apparatus is optimum as an alternative of two-dimensional array LED modules for traffic signal devices. At 25° C or higher, LEDs have an allowable current lowered and produce low luminance.

The display apparatus and the method of driving same according to the present invention are not limited to the above embodiments, but may be embodied in various arrangement without departing from the scope of the present invention.